WHAT IS CLAIMED IS:

1. For use in an instruction queue having a plurality of instruction slots, a mechanism for queueing and retiring instructions, comprising:

a plurality of tag fields corresponding to said plurality of instruction slots;

control logic, coupled to said tag fields, that assigns tags to said tag fields to denote an order of instructions in said instruction slots; and

a tag multiplexer, coupled to said control logic, that changes said order by reassigning only said tags.

2. The mechanism as recited in Claim 1, further comprising loop detection logic, coupled to said control logic, that prevents ones of said instructions that are in a loop from being retired.

3. The mechanism as recited in Claim 1, further comprising an input ordering multiplexer coupled to said control logic and to said plurality of instruction slots and configured to write said instructions into said plurality of instruction slots.

4. The mechanism as recited in Claim 1, further comprising

an output ordering multiplexer coupled to said control logic and to said plurality of instruction slots and configured to retire ones of said instructions.

5. The mechanism as recited in Claim 1 wherein said instruction slots number six and said tags number six.

6. The mechanism as recited in Claim 1 wherein said control logic further determines an order of at least one new instruction and causes said at least one new instruction to be written into at least one of said plurality of instruction slots.

7. The mechanism as recited in Claim 1 wherein said control logic retires all of said instructions in response to receipt of a mispredict signal.

8. For use in an instruction queue having a plurality of instruction slots, a method for queueing and retiring instructions, comprising:

providing a plurality of tag fields corresponding to said plurality of instruction slots;

assigning tags to said tag fields to denote an order of instructions in said instruction slots; and

changing said order by reassigning only said tags.

9. The method as recited in Claim 8, further comprising preventing, with loop detection logic, ones of said instructions that are in a loop from being retired.

10. The method as recited in Claim 8, further comprising writing said instructions into said plurality of instruction slots with an input ordering multiplexer coupled to said control logic and to said plurality of instruction slots.

11. The method as recited in Claim 8, further comprising retiring said at least one of said instructions with an output ordering multiplexer coupled to said control logic and to said plurality of instruction slots.

12. The method as recited in Claim 8 wherein said instruction slots number six and said tags number six.

13. The method as recited in Claim 8 further comprising determining an order of at least one new instruction and causing said at least one new instruction to be written into at least one of said plurality of instruction slots.

14. The method as recited in Claim 8 further comprising retiring all of said instructions in response to receipt of a mispredict signal.

15. A digital signal processor (DSP), comprising:

a pipeline having stages;

an issue unit including an instruction queue having a plurality of instruction slots;

a plurality of tag fields corresponding to said plurality of instruction slots;

control logic, coupled to said tag fields, that assigns tags to said tag fields to denote an order of instructions in said instruction slots; and

a tag multiplexer, coupled to said control logic, that changes said order by reassigning only said tags.

16. The DSP as recited in Claim 15, further comprising loop detection logic, coupled to said control logic, that prevents ones of said instructions that are in a loop from being retired.

17. The DSP as recited in Claim 15, further comprising an input ordering multiplexer coupled to said control logic and to said plurality of instruction slots and configured to write said instructions into said plurality of instruction slots.

18. The DSP as recited in Claim 15, further comprising an output ordering multiplexer coupled to said control logic and to

said plurality of instruction slots and configured to retire at least one of said instructions.

19. The DSP as recited in Claim 15 wherein said instruction slots number six and said tags number six.

20. The DSP as recited in Claim 15 wherein said control logic further determines an order of at least one new instruction and causes said at least one new instruction to be written into at least one of said plurality of instruction slots.

21. The DSP as recited in Claim 15 wherein said control logic retires all of said instructions in response to receipt of a mispredict signal.